THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SCOTT H. PRENGLE and
ROBERT H. EKLUND

Appeal No. 95-4174
Application 08/165,553[1]

ON BRIEF

Before THOMAS, HAIRSTON, and KRASS, Administrative Patent Judges.

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[1] Application for patent filed December 10, 1993. According to appellants, the application is a continuation of Application 07/895,535, filed June 8, 1992; which is a division of Application 07/785,174, filed October 29, 1991, now Patent No. 5,171,702; which is a continuation of Application 07/383,960, filed July 21, 1989, now abandoned.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 14 through 21. Claims 1 through 13 have been canceled.

The invention pertains to a BiCMOS structure having a thick dielectric layer to reduce emitter-base capacitance in bipolar transistors.

Independent claim 14 is reproduced as follows:

14. A single polysilicon layer BiCMOS structure at a semiconductor surface of a body, comprising:

a bipolar transistor, comprising:

a collector region of a first conductivity type and having a first impurity concentration;

an intrinsic base region of a second conductivity type disposed at said semiconductor surface and within said collector region;

an emitter region of said first conductivity type disposed at said semiconductor surface and within said intrinsic base region;

a thick dielectric layer, directly adjacent said intrinsic base region and having a contact therethrough to said emitter region; and

an emitter electrode, disposed over said thick dielectric layer such that said thick dielectric layer separates said emitter electrode from said intrinsic base

region, wherein said emitter electrode is in contact with said emitter region through said contact;

an insulated-gate field effect transistor, comprising:

a well region of said first conductivity type and having said first impurity concentration;

a gate dielectric comprising thermal silicon dioxide of a thickness substantially thinner than a thickness of said thick dielectric layer of said bipolar transistor, disposed over a portion of said well region;

a gate electrode disposed over said well region and insulated therefrom by said gate electric [sic, dielectric]; and

source drain regions of said second conductivity type and having a second impurity concentration disposed at said semiconductor surface on both lateral sides of said gate electrode and within said well region; and

an isolation structure disposed at said semiconductor surface between said bipolar transistor and said insulated-gate field effect transistor.

The examiner relies on the following references:

Homma et al. (Homma)	4,735,916	Apr. 5, 1988
Schaber et al. (Schaber)	4,737,472	Apr. 12, 1988
Maeda et al. (Maeda)	4,931,407	Jun. 5, 1990
Soejima	4,957,874	Sep. 18, 1990
Uchida et al. (Uchida)	5,214,302	May 25, 1993

Claims 14 through 21 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the invention. Claims 14 and 21 stand rejected under 35 U.S.C. § 102(e) as alternatively anticipated by either Soejima or Maeda. Claims 14 and 21 also stand rejected under 35 U.S.C. § 102(b) as anticipated by Homma. Claims 14 through 19 also stand rejected under 35 U.S.C. 102(b) as anticipated by Schaber. Finally, claims 14 through 21 stand rejected under
35 U.S.C. § 103 as unpatentable over Uchida and Homma.

Reference is made to the brief and answer for the respective positions of appellants and the examiner.

OPINION

Turning first to the rejection of claims 14 through 21 under 35 U.S.C. § 112, second paragraph, we will not sustain this rejection.

The examiner takes the position that the phrase “a single-polysilicon layer BiCMOS structure at a semiconductor surface of a body” is misdescriptive because there are two

polysilicon layers, 68 and 72, formed at two different manufacturing steps, as disclosed by the specification.

The examiner appears to be concerned with the process of making the BiCMOS structure while the claim is directed to a final structure of the BiCMOS shown in Figures 1 and 5. No matter how many manufacturing steps there are in the process, the final structure to which the claimed invention is directed is a "single-polysilicon layer BiCMOS." As appellants point out [brief-page 5], this is a term of art well known in the art of semiconductor devices, i.e., a BiCMOS device having only one distinct polysilicon layer. The single polysilicon layer in the finished structure is shown at 72 in Figure 1, for example. The polysilicon layer 68, referred to by the examiner, is no longer a separate entity in the final structure, having been merged with polysilicon layer 72 during the manufacturing process [see page 20, lines 23-26 of the specification]. The examiner has not convinced us that there is anything unclear or indefinite about the claimed "single-polysilicon layer BiCMOS structure."

We now turn to the rejections of claims 14 and 21 under

35 U.S.C. § 102(b) as anticipated by Homma, of claims 14 through 19 under 35 U.S.C. § 102(b) as anticipated by Schaber, and of claims 14 and 21 under 35 U.S.C. § 102(e) as anticipated by Soejima. We will not sustain these rejections because, as appellants point out, Homma, Schaber and Soejima are not directed to a "single polysilicon layer BiCMOS structure," as claimed. The examiner does not deny this but prefers to ignore this limitation because it appears in the preamble and the "preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause," citing Kropa v. Robie, 187 F.2d 150, 88 USPQ 478 (CCPA 1951). [answer-page 14].

We disagree with the examiner. The recitation in the preamble of "A single polysilicon layer BiCMOS structure" gives "life and meaning" to the body of the claim because it sets forth the parameters in which the rest of the structure

must exist, i.e., the structure recited must not be in a double-polysilicon layer device.

Since neither Homma nor Schaber nor Soejima teaches or suggests each and every element of the claimed invention, we will not sustain the rejection of claims 14 through 21 under 35 U.S.C. § 102(b) based on Homma (claims 14 and 21) or Schaber (claims 14 through 19) or the rejection of claims 14 and 21 under 35 U.S.C. § 102(e) based on Soejima.

Turning to the rejection of claims 14 and 21 under 35 U.S.C. § 102(e) over Maeda, we will sustain this rejection.

The examiner details the rejection and how the claimed elements are met by Maeda at page 8 of the answer. Appellants agree that Maeda does, indeed, teach a single polysilicon layer BiCMOS structure [pages 9-10 of the brief]. Appellants argue only that, in Maeda, the dielectric layer and the gate dielectric are the same and so there is no teaching in Maeda that the dielectric layer between the emitter electrode and the intrinsic base region is different, in thickness, from the gate dielectric layer.

The examiner points out, however, that in Figures 1H and 1I of Maeda, the "thick dielectric layer" 35 is indicated to be 2000 angstroms thick [column 4, line 54] while gate dielectric 23 is indicated to be about 150 angstroms thick [column 4, lines 7 et seq.], which is "substantially thinner" than the thickness of the thick dielectric layer. The examiner's position appears to be reasonable to us and appellants have never refuted the examiner's identification of element 23 in Maeda as the claimed "gate dielectric" and of element 35 in Maeda as the claimed "thick dielectric layer," nor have appellants submitted a reply brief refuting the examiner's response that Maeda's gate dielectric 23 is of a thickness (150 angstroms) "substantially thinner than the thickness of said thick dielectric layer" 35 (2000 angstroms).

Accordingly, in our view, the examiner has established a prima facie case of anticipation which has not been successfully rebutted by appellants. Consequently, we will sustain the rejection of claims 14 and 21 under 35 U.S.C. § 102(e) as anticipated by Maeda.

We turn, finally, to the rejection of claims 14 through 21 under 35 U.S.C. § 103 as unpatentable over Uchida in view of Homma. We will not sustain this rejection for the reasons, supra, with regard to the rejections relying on Homma, Schaber and Soejima. That is, neither Uchida nor Homma is directed to a single polysilicon layer BiCMOS structure and the examiner does not deny this. The examiner merely wants to ignore this limitation because it appears in the preamble. As indicated supra, it is our view that this recitation breaths life and meaning into the claim and is a specific claim limitation which cannot be ignored. Accordingly, since neither Uchida nor Homma teaches or suggests this limitation, the claimed subject matter cannot be considered obvious, within the meaning of 35 U.S.C. § 103.

We have not sustained the rejections of claims 14 through 21 under either 35 U.S.C. § 112, second paragraph, or 35 U.S.C. § 103. We have also not sustained the rejection of claims 14 and 21 under 35 U.S.C. § 102 over either Homma or Soejima. Nor have we sustained the rejection of claims 14 through 19 under 35 U.S.C. § 102(b) over Schaber. We

have, however, sustained the rejection of claims 14 and 21 under 35 U.S.C. § 102(e) as anticipated by Maeda.

Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS Administrative Patent Judge	)	
KENNETH W. HAIRSTON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
ERROL A. KRASS Administrative Patent Judge	)	

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